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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/211,677	12/14/98	LEE H	8733D-7153

EXAMINER	
NGUYEN, K	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/211,677	LEE, HYUN CHANG	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 7/13/2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/211677 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusafuka et al (5,995,074).

As to claims 1-6, Kusafuka teaches a TFT LCD which includes the waveforms having a gate signal 22 is input to a gate line Gn corresponding to the claimed the first

gate voltage and Gn+1 corresponding to the claimed the second gate voltage (see Fig. 5A, 5B), and liquid crystal potential corresponding to the claimed changes prior to exciting of successive gate signal lines (see Fig. 5C). It would have been obvious to a person of ordinary skill in the art to recognize that Kusafuka discloses a first gate voltage change prior to exciting of successive gate signal lines as claimed (by virtue of the operation described at Fig. 5A, 5B, 5C, col. 2, lines 42 to col. 3, lines 42).

As to claims 2-5, Kusafuka teaches a first gate voltage wave form Gn, Gn+1 and liquid crystal potential drop prior to exciting of the successive gate signal lines, drops exponentially, drops linearly, and drops stepwise (see Fig. 5A, 5B, 5C).

As to claim 6, Kusafuka teaches a minimum value of the first gate voltage Gn is higher than a maximum value of the second gate voltage Gn+1 (see Fig. 5A, 5B, 5C).

5. Claims 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusafuka et al in view of Yasui et al (5,784,039).

As to claims 7-9, Kusafuka et al teaches all of the claimed limitations of claim 1, except for a gate driver connected to the gate lines and having a shift resister.

However, Yasui teaches a related an active matrix LCD apparatus which includes a method comprising the steps of: a liquid crystal pixels L_{ij} (fig.1B, col. 4, lines 35-36) having switching transistors Q_{ij} and $Q_{i+1,,j}$

a source driver 2 (data driver) has connected thereto n column of source buses S_i-S_n corresponding to the claimed a plurality of data signal lines each connected to the first electrode associated with any one of the transistors (fig.1A, col. 4, lines 31-32).

a gate driver 3 (shift register) has connected thereto m+1 rows of gate buses G_1-G_{m+1} corresponding to the claimed a plurality of gate signal line each connected to the gate electrode associated with any one of the transistors (fig.1A, col.4, lines 32-33).

the gate driver 3 supplied the gate buses G_1, G_2, ..., G_{m+1} one after another with pulse-like scanning (referred to also as gate bus drive voltages or simply as gate voltage) voltages V_{G1}, V_{G2} ... V_{Gm+1} (col. 4, lines 53-56). By this, TFTs on each row are sequentially selected and turned ON is a diagram showing an equivalent circuit of the pixel in one mesh in Fig.1B (col. 4, lines 60-62).

in the subsequent period $t_0<t<t_1$ the TFT on the i-th row is turned ON by the select pulse P_g and new data is written by the source voltage V_s (Fig.3A, col. 6, lines 1-3). In the period $t_1<t<t_2$, since the TFT on the i-th row is turned OFF with V_s-dV_p (Fig. 3B, col. 6, lines 45-47).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to utilize the gate driver 3 circuit taught by Yasui et al for the gate wiring side driver circuit G1, G2,..., Gn disclosed in the active matrix display system of Kusafuka et al because this would reduce flicker in the LCD (see abstract of Yasui et al).

As to claim 12, Yasui teaches Vc (5) is ground (see Fig. 1A).

As to claim 10, 11 and 13-15, Yasui teaches in the subsequent period $t_0<t<t_1$ the TFT on the i-th row is turned ON by the select pulse P_g and new data is written by the source voltage V_s (Fig.3A, col. 6, lines 1-3). In the period $t_1<t<t_2$, since the TFT on the i-th row is turned OFF with V_s-dV_p (Fig. 3B, col. 6, lines 45-47). It would have been

obvious to a person of ordinary skill in the art to recognize that Yasui discloses claim 10 recites "a high level gate voltage generator .....of successive gate signal lines as claimed.

As to claims 16-20, Yasui teaches an active matrix liquid crystal display apparatus which includes a liquid crystal pixels L_{ij} (fig.1B, col. 4, lines 35-36) having switching transistors Q_{ij} and $Q_{i+1,,j}$

a source driver 2 (data driver) has connected thereto n column of source buses S_i-S_n corresponding to the claimed a plurality of data signal lines each connected to the first electrode associated with any one of the transistors (fig.1A, col. 4, lines 31-32).

a gate driver 3 (shift register) has connected thereto m+1 rows of gate buses G_1-G_{m+1} corresponding to the claimed a plurality of gate signal line each connected to the gate electrode associated with any one of the transistors (fig.1A, col.4, lines 32-33).

the gate driver 3 supplied the gate buses G_1, G_2, ..., G_{m+1} one after another with pulse-like scanning (referred to also as gate bus drive voltages or simply as gate voltage) voltages V_{G1}, V_{G2} ... V_{Gm+1} (col. 4, lines 53-56). By this, TFTs on each row are sequentially selected and turned ON is a diagram showing an equivalent circuit of the pixel in one mesh in Fig.1B (col. 4, lines 60-62).

in the subsequent period $t_0<t<t_1$ the TFT on the i-th row is turned ON by the select pulse P_g and new data is written by the source voltage V_s (Fig.3A, col. 6, lines 1-3). In the period $t_1<t<t_2$, since the TFT on the i-th row is turned OFF with V_s-dV_p (Fig. 3B, col. 6, lines 45-47).

It would have been obvious to a person of ordinary skill in the art to recognize that Yasui discloses claim 16 recites "a liquid crystal display (LCD) device, comprising: .....a successive scanning line" as claimed (by virtue of the operation described at col. 4, lines 25 to col. 5, col. 6, lines 67).

Response to Arguments

6. Applicant's arguments filed 7/13/2001 have been fully considered but they are not persuasive.

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 703-305-6209. The examiner can normally be reached on MON-FRI from 9:00-5:00 with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A Hjerpe can be reached on 703-305-4709. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-306-0377 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Kevin M. Nguyen
Examiner
Art Unit 2674

KN
August 10, 2001

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800